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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/905,516	Applicant(s) AVERY, JAMES M.	
	Examiner Christopher E. Lee	Art Unit 2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 May 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-14, 16-46 and 48-50 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-14, 16-46 and 48-50 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Receipt Acknowledgement

1. Receipt is acknowledged of the Amendment filed on 17th of May 2004. Claims 1, 7, 16, 22, 29, 30, 35, 37, 42, 44 and 48 have been amended; claims 15 and 47 have been canceled; and no claim has been newly added since the Non-Final Office Action was mailed on 20th of February 2004. Currently, claims 1-14, 16-46 and 48-50 are pending in this application.

Specification

2. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required:

10 In the claims 32-34 and 39-41, they recite that the act of detecting the presence of the switch in the claims 32 and 39, the act of determining the number of primary ports present in the switch in the claims 33 and 40, and the act of storing the value in the claims 34 and 41 include issuing a configuration transaction, respectively. However, the specification fails to provide proper basis for the claimed limitations (See Application, pages 2-4).

Claim Objections

15 3. Claim 46 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. In the claim 46, it recites the limitation "receiving the type1 configuration transaction in an HT switch" in lines 2-3. However, its prior claim 44 already limits the scope of the claimed invention, such that the subject matter "HT switch" is an HT(HyperTransport switch) in line 6.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

25 The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it

pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 32-34 and 39-41 are rejected under 35 U.S.C. 112, first paragraph, because the
5 specification, while being enabling for issuing a configuration transaction (See Application, pages 2-4), does not reasonably provide enablement for issuing a configuration transaction included in the method steps of detecting the presence of the switch (See Claims 32 and 39), determining the number of primary ports present in the switch (See Claims 33 and 40), and/or storing the value (See Claims 34 and 41). The specification does not enable any person skilled in the art to which it pertains, or with which it is most
10 nearly connected, to make/use the invention commensurate in scope with these claims.

In fact, the disclosed invention states that the method of storing information in a configuration register (See Application, page 2, line 23), the method of retrieving information from a configuration register (See Application, page 3, line 8), and the method of forwarding a configuration transaction (See Application, page 4, lines 13-14) include the step of issuing a configuration transaction. However, any method step
15 (i.e., the act of performing) of the Applicant's disclosed invention does not include the step of issuing a configuration transaction. The Examiner doubts how the steps of detecting the presence of the switch, determining the number of primary ports present in the switch, and/or storing the value could include the method step of issuing a configuration transaction in light of the specification.

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

20 The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 7, 8, 22, 23, 27, 31, 35 and 36 are rejected under 35 U.S.C. 112, second paragraph, as
being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant
25 regards as the invention.

The claims 7, 8, 22, 23, recite the limitation "the first switch" in line 2, respectively. There is insufficient antecedent basis for this limitation in the claims, respectively. Therefore, the term "the first switch" could be considered as --the first HT switch-- since it is not clearly defined in the claims.

The claim 27 recites the limitation "the second switch" in line 2. There is insufficient antecedent basis for this limitation in the claim. Therefore, the term "the second switch" could be considered as --the second HT switch-- since it is not clearly defined in the claims.

The claims 31, 35 and 36 recite the limitation "the switch" in line 2 of the claim 31 and 35, in line 3 of the claim 36, respectively. There is insufficient antecedent basis for this limitation in the claims, respectively. Therefore, the term "the switch" could be considered as --the HT switch-- since it is not clearly defined in the claims.

8. Claims 32, 33, 39 and 40 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01.

In the specification, on page 12, lines 17-21, it discloses (1-a) issuing a type 0 configuration read transaction, (1-b) retrieving information from configuration registers located within HT I/O devices, and (1-c) the retrieved information including the capabilities of the first HT switch, which indicate that an HT switch is coupled to I/O bus. However, the claims 32 and 39 respectively omits the steps of retrieving information from configuration registers located within HT I/O devices, which is an essential step of the disclosed invention in the specification since the presence of the switch could be detected after performing the step of retrieving the capabilities of the switch.

Furthermore, it discloses (2-a) issuing a type 0 configuration read transaction, (2-b) retrieving information including the number of ports in the first HT switch. However, the claims 33 and 40 respectively omits the steps of retrieving the number of ports in the first HT switch, which is an essential step of the disclosed invention in the specification since the number of primary ports present in the switch could be determined after performing the step of retrieving the information.

Claim Rejections - 35 USC § 103

9. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

10. Claims 1, 2, 4-14, 16, 17, 19-31, 35-38, 42-46 and 48-50 are rejected under 35 U.S.C. 103(a) as
5 being unpatentable over PCI-to-PCI Bridge Architecture Specification [published by PCI Special Interest Group, on 18th of December 1998; cited by the Applicant; hereinafter PCI-to-PCI Bridge] in view of Applicant Admitted Prior Art [hereinafter AAPA].

Referring to claim 1, PCI-to-PCI Bridge discloses a method (i.e., a method of configuration transaction; See Chapter 3. Configuration), performed by a computer system (i.e., typical bridge
10 application in Fig. 1-1) that includes a host processor (i.e., CPU in Fig. 1-1) coupled to a first bus (i.e., Host Bus in Fig. 1-1), a first switch (i.e., Host Bridge in Fig. 1-1) coupled to said first bus and a second bus (i.e., PCI Bus 0 in Fig. 1-1), a second switch (i.e., PCI-PCI Bridge 1 in Fig. 1-1) coupled to said second bus and a third bus (i.e., PCI Bus 1 in Fig. 1-1), and a device (i.e., PCI Device in Fig. 1-1) coupled to said third bus, of storing information (i.e., being performed by Configuration Write transaction; See
15 page 20, 3.1.1. Type 0 Configuration Transaction Support) in a configuration register (i.e., Configuration Registers in Fig. 3-2; See page 25, 3.2. PCI-to-PCI Bridge Configuration Space Header Format) in said device, the method comprising: issuing (i.e., issued by configuration software executed by said host processor i.e., CPU) a first configuration transaction (i.e., Type 1 Configuration Transaction) onto said first bus (i.e., Host Bus); forwarding said first configuration transaction to said second bus (See page 23,
20 3.1.2.1.2. Type 1 to Type 1 Forwarding); translating (i.e., converting) said first configuration transaction (i.e., Type 1 Configuration Transaction) into a second configuration transaction (i.e., Type 0 Configuration Transaction); forwarding said second configuration transaction to said third bus (See page 21, 3.1.2.1.2. Type 1 to Type 0 Conversion); and storing information in said configuration register (See

page 25, 3.2. PCI-to-PCI Bridge Configuration Space Header Format; writing configuration information into said configuration register by Configuration Write PCI Bus transaction).

PCI-to-PCI Bridge does not expressly teach said first and second switches are HT switches.

AAPA discloses a HyperTransport ("HT") I/O interconnect structure (See page 1, lines 17-22), wherein

5 an HT switch handles multiple HT I/O data streams and managing the interconnection between attached HT I/O devices in said HT I/O interconnect structure (See page 2, lines 13-14).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have applied said HT switch, as disclosed by AAPA, for said first and second switches, as

disclosed by PCI-to-PCI Bridge, for the advantage of providing a significant increase in transaction

10 throughput over existing I/O bus architectures such as PCI and AGP (See AAPA, page 1, lines 19-22).

Referring to claim 2, PCI-to-PCI Bridge teaches the act of issuing said first configuration transaction (i.e., Type 1 Configuration Transaction) includes a host processor (i.e., CPU in Fig. 1-1) issuing said first configuration transaction (i.e., issued by configuration software executed by said CPU; See Chapter 3. Configuration).

15 *Referring to claim 4*, PCI-to-PCI Bridge teaches the act of issuing said first configuration transaction (i.e., Type 1 Configuration Transaction) includes issuing a type1 configuration transaction (See page 20, 3.1.2. Type 1 Configuration Transaction Support).

Referring to claim 5, PCI-to-PCI Bridge teaches the act of issuing said first configuration transaction (i.e., Type 1 Configuration Transaction) includes issuing said first configuration transaction
20 (i.e., issued by configuration software executed by said CPU; See Chapter 3. Configuration) onto a bus (i.e., PCI Bus 2 in Fig. 1-1) that is coupled to a third switch (i.e., PCI-PCI Bridge 2 in Fig. 1-1).

Referring to claim 6, PCI-to-PCI Bridge teaches the act of issuing said first configuration transaction (i.e., Type 1 Configuration Transaction) includes issuing said first configuration transaction

(i.e., issued by configuration software executed by said CPU; See Chapter 3. Configuration) onto a bus (i.e., PCI Bus 2 in Fig. 1-1) that is coupled to an I/O device (i.e., PCI Device in Fig. 1-1).

Referring to claim 7, PCI-to-PCI Bridge, as modified by AAPA, teaches the act of issuing said first configuration transaction (i.e., Type 1 Configuration Transaction; PCI-to-PCI Bridge) includes
5 *issuing a first configuration (See PCI-to-PCI Bridge, Chapter 3. Configuration) to said first HT switch (i.e., HyperTransport switch; AAPA).*

Referring to claim 8, PCI-to-PCI Bridge, as modified by AAPA, teaches the act of forwarding said first configuration transaction (i.e., Type 1 Configuration Transaction; PCI-to-PCI Bridge) includes said first HT switch (i.e., HyperTransport switch; AAPA) forwarding said first configuration transaction
10 *(i.e., forwarding type 1 configuration transaction to secondary interface; See PCI-to-PCI Bridge, page 23, 3.1.2.1.2. Type 1 to Type 1 Forwarding).*

Referring to claim 9, PCI-to-PCI Bridge teaches the act of forwarding said first configuration transaction (i.e., Type 1 Configuration Transaction) includes forwarding a type1 configuration transaction (i.e., forwarding type 1 configuration transaction to secondary interface; See page 23, 3.1.2.1.2. Type 1 to
15 *Type 1 Forwarding).*

Referring to claim 10, PCI-to-PCI Bridge teaches the act of translating (i.e., converting) said first configuration transaction (i.e., Type 1 Configuration Transaction) into a second configuration transaction (i.e., Type 0 Configuration Transaction) includes translating a type1 configuration transaction into a type0 configuration transaction (See page 21, 3.1.2.1.2. Type 1 to Type 0 Conversion).

20 *Referring to claim 11, PCI-to-PCI Bridge teaches the act of storing information includes storing a primary-segment number (i.e., Primary Bus Number in Fig. 3-2; See page 40, 3.2.5.2. Primary Bus Number Register).*

Referring to claim 12, PCI-to-PCI Bridge teaches the act of storing information includes storing a secondary-segment number (i.e., Secondary Bus Number in Fig. 3-2; See page 40, 3.2.5.3. Secondary Bus Number Register).

Referring to claim 13, PCI-to-PCI Bridge teaches the act of storing information includes storing a
5 Unit ID (i.e., Device ID in Fig. 3-2; See page 26, 3.2.4.2. Device ID Register).

Referring to claim 14, PCI-to-PCI Bridge teaches said first configuration transaction (i.e., Type 1 Configuration Transaction) contains a primary-segment field (i.e., Device Number AD[15::11] for Type 1 in Fig. 3-1) and a secondary-segment field (i.e., Bus Number AD[23::16] for Type 1 in Fig. 3-1). Refer to pages 21-22; 3.1.2.1.1. Type 1 to Type 0 Conversion.

10 *Referring to claim 16*, PCI-to-PCI Bridge discloses a method (i.e., a method of configuration transaction; See Chapter 3. Configuration), performed by a computer system (i.e., typical bridge application in Fig. 1-1) that includes a host processor (i.e., CPU in Fig. 1-1) coupled to a first bus (i.e., Host Bus in Fig. 1-1), a first switch (i.e., Host Bridge in Fig. 1-1) coupled to said first bus and a second bus (i.e., PCI Bus 0 in Fig. 1-1), a second switch (i.e., PCI-PCI Bridge 1 in Fig. 1-1) coupled to said
15 second bus and a third bus (i.e., PCI Bus 1 in Fig. 1-1), and a device (i.e., PCI Device in Fig. 1-1) coupled to said third bus, of retrieving information (i.e., being performed by Configuration Read transaction; See page 20, 3.1.1. Type 0 Configuration Transaction Support) from a configuration register (i.e., Configuration Registers in Fig. 3-2; See page 25, 3.2. PCI-to-PCI Bridge Configuration Space Header Format) in said device, the method comprising: issuing (i.e., issued by configuration software executed
20 by said host processor i.e., CPU) a first configuration transaction (i.e., Type 1 Configuration Transaction) onto said first bus (i.e., Host Bus); forwarding said first configuration transaction to said second bus (See page 23, 3.1.2.1.2. Type 1 to Type 1 Forwarding); translating (i.e., converting) said first configuration transaction (i.e., Type 1 Configuration Transaction) into a second configuration transaction (i.e., Type 0 Configuration Transaction); forwarding said second configuration transaction to said third bus (See page

21, 3.1.2.1.2. Type 1 to Type 0 Conversion); and retrieving information in said configuration register (See page 25, 3.2. PCI-to-PCI Bridge Configuration Space Header Format; reading configuration information from said configuration register by Configuration Read PCI Bus transaction).

PCI-to-PCI Bridge does not expressly teach said first and second switches are HT switches.

- 5 AAPA discloses a HyperTransport ("HT") I/O interconnect structure (See page 1, lines 17-22), wherein an HT switch handles multiple HT I/O data streams and managing the interconnection between attached HT I/O devices in said HT I/O interconnect structure (See page 2, lines 13-14).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have applied said HT switch, as disclosed by AAPA, for said first and second switches, as
10 disclosed by PCI-to-PCI Bridge, for the advantage of providing a significant increase in transaction throughput over existing I/O bus architectures such as PCI and AGP (See AAPA, page 1, lines 19-22).

Referring to claim 17, PCI-to-PCI Bridge teaches the act of issuing said first configuration transaction (i.e., Type 1 Configuration Transaction) includes a host processor (i.e., CPU in Fig. 1-1) issuing the first configuration transaction (i.e., issued by configuration software executed by said CPU;
15 See Chapter 3. Configuration).

Referring to claim 19, PCI-to-PCI Bridge teaches the act of issuing said first configuration transaction (i.e., Type 1 Configuration Transaction) includes issuing a type1 configuration transaction (See page 20, 3.1.2. Type 1 Configuration Transaction Support).

Referring to claim 20, PCI-to-PCI Bridge teaches the act of issuing said first configuration
20 transaction (i.e., Type 1 Configuration Transaction) includes issuing said first configuration transaction (i.e., issued by configuration software executed by said CPU; See Chapter 3. Configuration) onto a bus (i.e., PCI Bus 2 in Fig. 1-1) that is coupled to a third switch (i.e., PCI-PCI Bridge 2 in Fig. 1-1).

Referring to claim 21, PCI-to-PCI Bridge teaches the act of issuing said first configuration transaction (i.e., Type 1 Configuration Transaction) includes issuing said first configuration transaction

(i.e., issued by configuration software executed by said CPU; See Chapter 3. Configuration) onto a bus (i.e., PCI Bus 2 in Fig. 1-1) that is coupled to an I/O device (i.e., PCI Device in Fig. 1-1).

Referring to claim 22, PCI-to-PCI Bridge, as modified by AAPA, teaches the act of issuing said first configuration transaction (i.e., Type 1 Configuration Transaction; PCI-to-PCI Bridge) includes issuing a first configuration (See PCI-to-PCI Bridge, Chapter 3. Configuration) to said first HT switch (i.e., HyperTransport switch; AAPA).

Referring to claim 23, PCI-to-PCI Bridge, as modified by AAPA, teaches the act of forwarding said first configuration transaction (i.e., Type 1 Configuration Transaction; PCI-to-PCI Bridge) includes said first HT switch (i.e., HyperTransport switch; AAPA) forwarding said first configuration transaction (i.e., forwarding type 1 configuration transaction to secondary interface; See PCI-to-PCI Bridge, page 23, 3.1.2.1.2. Type 1 to Type 1 Forwarding).

Referring to claim 24, PCI-to-PCI Bridge teaches the act of forwarding said first configuration transaction (i.e., Type 1 Configuration Transaction) includes forwarding a type1 configuration transaction (i.e., forwarding type 1 configuration transaction to secondary interface; See page 23, 3.1.2.1.2. Type 1 to Type 1 Forwarding).

Referring to claim 25, PCI-to-PCI Bridge teaches the act of translating (i.e., converting) said first configuration transaction (i.e., Type 1 Configuration Transaction) into a second configuration transaction (i.e., Type 0 Configuration Transaction) includes translating a type1 configuration transaction into a type0 configuration transaction (See page 21, 3.1.2.1.2. Type 1 to Type 0 Conversion).

Referring to claim 26, PCI-to-PCI Bridge teaches the act of retrieving (i.e., reading) said information (i.e., configuration information) includes sending said information (viz., reading the configuration information from the configuration register in the PCI device) to said host processor (i.e., CPU in Fig. 1-1; See page 20, 3.1.1. Type 0 Configuration Transaction Support - PCI Bus command is a Configuration Read or Configuration Write).

Referring to claim 27, PCI-to-PCI Bridge, as modified by AAPA, teaches the act of retrieving (i.e., reading; PCI-to-PCI Bridge) said information (i.e., configuration information; PCI-to-PCI Bridge) includes sending said information (viz., forwarding the configuration information from the configuration register in the PCI device; PCI-to-PCI Bridge) to said second HT switch (i.e., HyperTransport switch; AAPA; See PCI-to-PCI Bridge, page 24, 3.1.2.2.1. Type 1 to Type 1 Forwarding).

Referring to claim 28, PCI-to-PCI Bridge teaches the act of retrieving (i.e., reading) said information (i.e., configuration information) includes retrieving (i.e., reading) capabilities information (i.e., Capabilities Pointer in Fig. 3-2; See page 47, 3.2.5.12. Capabilities Pointer).

Referring to claim 29, PCI-to-PCI Bridge discloses a method (i.e., a method of configuration transaction; See Chapter 3. Configuration), performed by a computer system (i.e., typical bridge application in Fig. 1-1) that includes a host processor (i.e., CPU in Fig. 1-1) coupled to a bus (i.e., Host Bus in Fig. 1-1), and a switch (i.e., Host Bridge in Fig. 1-1) coupled to said bus, the method comprising: issuing (i.e., issued by configuration software executed by said host processor, i.e., CPU) a configuration transaction (i.e., Type 1 Configuration Transaction) that includes a primary-segment field (i.e., Device Number AD[15::11] for Type 1 in Fig. 3-1) and includes a secondary-segment field (i.e., Bus Number AD[23::16] for Type 1 in Fig. 3-1) onto said bus (See pages 21-22; 3.1.2.1.1. Type 1 to Type 0 Conversion); and receiving said configuration transaction in said switch (i.e., receiving the configuration transaction via Primary Interface of the Bridge; See page 20, 3.1.2.1. Primary Interface).

PCI-to-PCI Bridge does not expressly teach said switch is HT switch.

AAPA discloses a HyperTransport ("HT") I/O interconnect structure (See page 1, lines 17-22), wherein an HT switch handles multiple HT I/O data streams and managing the interconnection between attached HT I/O devices in said HT I/O interconnect structure (See page 2, lines 13-14).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have applied said HT switch, as disclosed by AAPA, for said switch, as disclosed by PCI-to-PCI

Bridge, for the advantage of providing a significant increase in transaction throughput over existing I/O bus architectures such as PCI and AGP (See AAPA, page 1, lines 19-22).

Referring to claims 30 and 37, PCI-to-PCI Bridge discloses a method (i.e., a method of slot numbering mechanism; See Chapter 13. Slot Numbering), performed by a computer system (i.e., typical bridge application in Fig. 1-1) that includes a host processor (i.e., CPU in Fig. 1-1) coupled to a bus (e.g., Bus 0-4 in Fig. 13-3), and a switch (i.e., PCI Bridges in Fig. 13-3) coupled to said bus, of generating a configuration-forwarding table (i.e., PCI-to-PCI Bridge Configuration in Fig. 3-2), the method comprising: detecting the presence of said switch (See page 145, 13.6. Run-Time Algorithm for Determining Chassis and Slot Number); determining the number of primary ports, which could be called secondary ports (i.e., # Slots in Fig. 13-3; See Table 3-10 on page 56) present in said switch (See page 140, 13.3. The Slot Number Register); for each primary port present in said switch (i.e., all slots presented by said bridges in Fig. 13-3), determining if said primary port is enabled or disabled (i.e., Slot Numbers 1-4 are enabled by PCI Bridge "A", Slot Numbers 5-7 are enabled by PCI Bridge "B", and Slot Numbers 8-10 are enabled by PCI Bridge "C" in Fig. 13-3); and for each enabled primary port (i.e., directly supported slots; e.g., Slot Numbers 1-4) in said switch (e.g., PCI Bridge "A"), storing a value (i.e., Secondary Bus Number) in said configuration-forwarding table that identifies a primary segment number, which could be called secondary segment number (i.e., Bus Number connected to the secondary interface of PCI-to-PCI Bridge) of said bus that is coupled to said port.

PCI-to-PCI Bridge does not expressly teach said first and second switches are HT switches.

PCI-to-PCI Bridge does not expressly teach said switch is HT switch.

AAPA discloses a HyperTransport ("HT") I/O interconnect structure (See page 1, lines 17-22), wherein an HT switch handles multiple HT I/O data streams and managing the interconnection between attached HT I/O devices in said HT I/O interconnect structure (See page 2, lines 13-14).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have applied said HT switch, as disclosed by AAPA, for said switch, as disclosed by PCI-to-PCI Bridge, for the advantage of providing a significant increase in transaction throughput over existing I/O bus architectures such as PCI and AGP (See AAPA, page 1, lines 19-22).

5 *Referring to claims 31 and 38*, PCI-to-PCI Bridge teaches storing a value (i.e., Subordinate Bus Number in Fig. 3-2; See page 40, 3.2.5.4. Subordinate Bus Number Register) that indicates that no segments are coupled to said disabled port (i.e., the range of bus numbers between the Secondary Bus Number and the Subordinate Bus Number indicating that slots for each disabled primary port in said HT switch (e.g., Slot Numbers 8-10) are subordinated behind a bridge (e.g., PCI Bridge "A"), but are not
10 directly connected to the bridge (i.e., PCI Bridge "A")).

Referring to claims 35, 36, 42 and 43, PCI-to-PCI Bridge, as modified by AAPA, teaches for each enabled primary port (i.e., directly supported slots; e.g., Slot Numbers 1-4; PCI-to-PCI Bridge) present in said HT switch (i.e., HyperTransport switch; AAPA; e.g., PCI Bridge "A"; PCI-to-PCI Bridge), storing a value (i.e., Secondary Bus Number; PCI-to-PCI Bridge) in said configuration-forwarding table
15 that indicates a span of the highest numbered segment, which is the highest numbered primary segment, that is coupled to said port of said HT switch (i.e., a number less than the bus number of the highest numbered PCI bus segment which is behind (subordinated to) the bridge; See PCI-to-PCI Bridge, page 40, 3.2.5.3. Secondary Bus Number Register and 3.2.5.4. Subordinate Bus Number Register).

Referring to claim 44, PCI-to-PCI Bridge discloses a method (i.e., a method of configuration
20 transaction; See Chapter 3. Configuration), performed by a computer system (i.e., typical bridge application in Fig. 1-1) that includes a host processor (i.e., CPU in Fig. 1-1) coupled to a first bus (i.e., Host Bus in Fig. 1-1), a first switch (i.e., Host Bridge in Fig. 1-1) coupled to said first bus and a second bus (i.e., PCI Bus 0 in Fig. 1-1), a second switch (i.e., PCI-PCI Bridge 1 in Fig. 1-1) coupled to said second bus, of forwarding a configuration transaction (See page 20, 3.1.2. Type 1 Configuration

Transaction Support) comprising: issuing (i.e., issued by configuration software executed by said host processor i.e., CPU) a type 1 configuration transaction (i.e., Type 1 Configuration Transaction) on said first bus (i.e., Host Bus); receiving said type 1 configuration transaction in said first switch (i.e., receiving the configuration transaction via Primary Interface of the Bridge; See page 20, 3.1.2.1. Primary Interface);

5 evaluating a logical equation (i.e., range checking of the bus number specified by address bits AD[23::16]); and if the result of said evaluation of said logical equation is a first value (i.e., if the bus number specified by address bits AD[23::16] is within the range of bus numbers between the Secondary Bus Number and the Subordinate Bus Number), then forwarding said type 1 configuration transaction to said second switch (See page 23, 3.1.2.1.2. Type 1 to Type 1 Forwarding).

10 PCI-to-PCI Bridge does not expressly teach said first and second switches are HT switches. AAPA discloses a HyperTransport ("HT") I/O interconnect structure (See page 1, lines 17-22), wherein an HT switch handles multiple HT I/O data streams and managing the interconnection between attached HT I/O devices in said HT I/O interconnect structure (See page 2, lines 13-14).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was
15 made to have applied said HT switch, as disclosed by AAPA, for said first and second switches, as disclosed by PCI-to-PCI Bridge, for the advantage of providing a significant increase in transaction throughput over existing I/O bus architectures such as PCI and AGP (See AAPA, page 1, lines 19-22).

Referring to claim 45, PCI-to-PCI Bridge teaches the act of evaluating a logical equation (i.e., bus range comparison) includes evaluating a first value from a configuration-forwarding table (i.e., the range
20 of bus numbers between the Secondary Bus Number and the Subordinate Bus Number from PCI-to-PCI Bridge Configuration Space).

Referring to claim 46, AAPA said first HT switch is an HT switch (i.e., HyperTransport switch; AAPA).

Referring to claim 48, PCI-to-PCI Bridge discloses a method (i.e., a method of configuration transaction; See Chapter 3. Configuration), performed by a computer system (i.e., typical bridge application in Fig. 1-1) that includes a host processor (i.e., CPU in Fig. 1-1) that is coupled to a first bus (i.e., Host Bus in Fig. 1-1), and a switch (i.e., Host Bridge in Fig. 1-1) that is coupled to said first bus, of forwarding a packet (See page 20, 3.1.2. Type 1 Configuration Transaction Support; i.e., forwarding a configuration transaction) comprising: receiving a packet (i.e., receiving type1 configuration transaction via Primary Interface of the Bridge; See page 20, 3.1.2.1. Primary Interface); determining a Unit ID (i.e., Bus Number in said type 1 configuration transaction in Fig. 3-1) of said packet (i.e., type 1 configuration transaction); retrieving a primary-segment value (i.e., Secondary Bus Number) from a first storage location (i.e., configuration register offset 19h) within said switch; d) retrieving a secondary-segment value (i.e., Subordinate Bus Number) from a second storage location (i.e., configuration register offset 1Ah) within said switch (See page 20, 3.1.2. Type 1 Configuration Transaction Support); and forwarding said packet (i.e., forwarding said type1 configuration transaction) through a port (i.e., Secondary Interface in Fig. 1-2) that is coupled to a bus (e.g., PCI Bus 0 in Fig. 1-1) that is identified by said primary-segment value and said secondary-segment value (i.e., identified after evaluating a logical equation, i.e., range checking if the bus number specified by address bits AD[23::16] is within the range of bus numbers between the Secondary Bus Number and the Subordinate Bus Number; See page 23, 3.1.2.1.2. Type 1 to Type 1 Forwarding).

PCI-to-PCI Bridge does not expressly teach said switch is HT switch.

AAPA discloses a HyperTransport ("HT") I/O interconnect structure (See page 1, lines 17-22), wherein an HT switch handles multiple HT I/O data streams and managing the interconnection between attached HT I/O devices in said HT I/O interconnect structure (See page 2, lines 13-14).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have applied said HT switch, as disclosed by AAPA, for said switch, as disclosed by PCI-to-PCI

Bridge, for the advantage of providing a significant increase in transaction throughput over existing I/O bus architectures such as PCI and AGP (See AAPA, page 1, lines 19-22).

Referring to claim 49, PCI-to-PCI Bridge teaches the act of retrieving said primary-segment (i.e., Secondary Bus Number) includes retrieving said primary-segment from a table (i.e., PCI-to-PCI Configuration table in PCI-to-PCI bridge; See Fig. 3-2) based upon said value of said Unit ID (i.e., Bus Number in said configuration transaction identifies the destination of said transaction; thus, said primary-segment, i.e., Secondary Bus Number, is retrieved from a PCI-to-PCI Bridge selected based on said Bus Number).

Referring to claim 50, PCI-to-PCI Bridge teaches the act of retrieving said secondary-segment (i.e., Subordinate Bus Number) includes retrieving said secondary-segment from a table (i.e., PCI-to-PCI Configuration table in PCI-to-PCI bridge; See Fig. 3-2) based upon said value of said Unit ID (i.e., Bus Number in said configuration transaction identifies the destination of said transaction; thus, said secondary-segment, i.e., Subordinate Bus Number, is retrieved from a PCI-to-PCI Bridge selected based on said Bus Number).

11. Claims 3 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over PCI-to-PCI Bridge in view of AAPA as applied to claims 1, 2, 4-14, 16, 17, 19-31, 35-38, 42-46 and 48-50 above, and further in view of McCoy [US 6,584,586 B1].

Referring to claims 3 and 18, PCI-to-PCI Bridge, as modified by AAPA, discloses all the limitations of the claims 3 and 18, respectively, except that does not teach the act of issuing said first configuration transaction includes issuing a HT configuration transaction.

McCoy discloses a capture and transport expansion card (CTC) for capturing and transferring internal system activity of a computer under test (See Abstract), wherein a CPU 102 of Fig. 2 performs the act of issuing a first configuration transaction (i.e., Configuration Transaction for PCI Bus Device CTC 114 in

Fig. 2), which is a HT configuration transaction (i.e., for configuring HT device (viz., Lightning Device Transport device CTC)).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said CTC device, as disclosed by McCoy, in said computer system, as disclosed by PCI-to-PCI Bridge, as modified by AAPA, for the advantage of providing tracks such internal activity as e.g., process flow, memory state, and bus activity, and exports a record of such internal activities to a separate system for the purpose of testing said computer system (See McCoy, col. 1, lines 8-14).

Response to Arguments

12. Applicant's arguments filed on 17th of May 2004 have been fully considered but they are not persuasive.

In response to the Applicant's argument with respect to the specification objection to as failing to provide proper antecedent basis for the claimed subject matter on Response page 12, line 1 through page 13, line 8, the Examiner respectfully disagrees.

The Applicant essentially asserts (1) the specification page 12, lines 6-18 supports for "detecting the presence of the switch" by "issuing a configuration transaction" as recited in claims 32 and 39, (2) the specification page 12, lines 17-21 supports for "determining the number of primary ports present in the switch" by "issuing a configuration transaction" as recited in claims 33 and 40, and (3) the specification page 12, lines 14-16 supports for "storing the value" by "issuing a configuration transaction" as recited in claims 34 and 41.

However, in contrary to the Applicant's statement, (1) the claims 32 and 39 do not recite "detecting the presence of the switch by issuing a configuration transaction", respectively, (2) the claims 33 and 40 do not recite "determining the number of primary ports present in the switch by issuing a configuration transaction", respectively, and (3) the claims 34 and 41 do not recite "storing the value by issuing a configuration transaction", respectively.

In fact, the Applicant recites (1) the limitation “detecting the presence of the switch includes issuing a configuration transaction” in the claims 32 and 39, respectively, (2) the claims 33 and 40 do not recite “determining the number of primary ports present in the switch by issuing a configuration transaction”, respectively, and (3) the claims 34 and 41 do not recite “storing the value by issuing a configuration transaction”, respectively. However, the Examiner doubts how the steps of detecting the presence of the switch, determining the number of primary ports present in the switch, and/or storing the value could include the method step of issuing a configuration transaction in light of the specification. Instead, the steps of detecting the presence of the switch, determining the number of primary ports present in the switch, and/or storing the value are performed after issuing a configuration transaction in light of the specification, and thus the steps of detecting the presence of the switch, determining the number of primary ports present in the switch, and/or storing the value do not include issuing a configuration transaction, but issuing a configuration transaction should be performed before the steps of detecting the presence of the switch, determining the number of primary ports present in the switch, and/or storing the value in light of the specification.

Thus, the Applicant’s argument on this point is not persuasive.

13. Applicant's arguments with respect to claims 1, 2, 4-14, 16, 17, 19-31, 35-38, 42-46 and 48-50 have been considered but are moot in view of the new ground(s) of rejection.

In response to the Applicant’s arguments with respect to the claimed subject matter “switch ” is a HT (HyperTransport) switch (See the exemplary claim 1), the Examiner brought AAPA reference in the rejection for the limitation which is not provided by PCI-to-PCI Bridge (See Claim Rejections under 35 USC § 103).

Conclusion

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

5 A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of
10 the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 703-305-5950. The examiner can normally be reached on 9:00am - 5:00pm.

15 If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained
20 from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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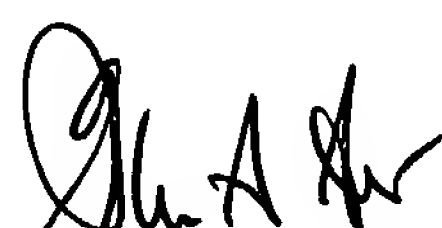
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Final Office Action

Christopher E. Lee
Examiner
Art Unit 2112

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